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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,888	08/30/2001	Konstantinos Manetakis	010186	2078

7590 01/23/2003

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EXAMINER

NGUYEN, LINH V

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 01/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/943,888	MANETAKIS, KONSTANTINOS	
	<b>Examiner</b>	<b>Art Unit</b>	
	Linh V Nguyen	2819	

*This communication appears on the cover sheet with the correspondence address --*

### Period for Reply

**THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.

- ## Status

- ## Disposition of Claims

- ## Application Papers

- Priority under 35 U.S.C. §§ 119 and 120**

- Attachment(s)**

- Part of Paper No. 2

## DETAILED ACTION

### *Drawings*

1. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 8, 10, 11, 12, 17, 18, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. US. Patent No. 5,223,753.

4. Regarding to claim 1, 10, and 18, Fig. 2 et al. disclose a amplifier circuit comprising: first (1), second (2), third (3), and fourth (12,13) MOS transistor devices configured in a translinear loop (no metes and bounds because the claimed does not have any structures or elements to describing this configuration), the first MOS device carrying a first control current (out put current of 1), the second MOS device carrying a second control current (output current of 2), the third MOS device carrying a current (current going through 3)) equal to the sum of the first and second control currents, and the fourth MOS device carrying a bias current (IX, IY); a first output circuit (11) coupled to a first voltage supply (VSS) and (drain of 11), the first output circuit sourcing a first

output current based on the first control current (current mirror of 1); and a second output circuit (10) coupled to a second voltage supply (VDD) and the output node, the second output circuit sourcing a second output current (current mirror of 2)) based on the second control currents (Current mirror I17, I18).

5. Regarding to claims 2 and 11, wherein the first and second output circuits are current mirrors and the first and second output currents equal the first and second control currents respectively (I10 current mirror of output current 2, I11 current mirror of output current 2).
6. Regarding to claims 3 and 12, wherein the MOS devices are NMOS devices (Fig. 2).
7. Regarding to claims 8 and 20, wherein a quiescent current of the Output stage is set by the bias control current (IX, IY), the bias current being increased above a selected predetermined level to lower a distortion level of the circuit (Col. 3 lines 65 – 68).
8. Regarding to claim 17, wherein the first and second output circuits comprise first and second output MOS devices, respectively, the maximum output voltage range at the output node being substantially equal to the difference between the first and second voltage supplies minus a saturation voltage of the first and second MOS output devices (inherent to Fig. 2).
9. Regarding to claim 19, wherein the source of the second MOS and third and MOS (2, 3) devices are coupled to a bias voltage (Vss, 3 directly connected to Vss, and 2 coupled to Vss through 3).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 4, and 13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claim 1, and 10 above, and further in view of 6,437,612, or 6,414,552, or 5,631,607, or 5,856,749, or 5,734,297 or 5,561,396.

12. Regarding to claim 4, and 13, As discussed above Lee et al. disclose every aspect of applicant's claimed invention, but does not explicitly disclose wherein the MOS devices operate in weak inversion mode. However weak-inversion mode are well-known art and a matter of design choice to have MOS devices operate in weak-inversion mode as have taught by many cited arts indicated above. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have MOS devices of Lee et al. amplifier operate in weak-inversion mode, which has taught by '612' ----'906'.

13. Claims 5, 6, 9, 14, 15, 16, 21 and 22, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claims 1, 8, 10, and 20 above.

14. Regarding to claims 5, 6, 14, 15, and 16, Lee et al. do not explicitly wherein further comprising a supply voltage having a voltage lower than  $2 * V_{GS} + V_{DS}^{sat}$  to provide the first voltage supply, or a supply voltage having a voltage equal to  $V_{GS} + 2*$

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$V_{DS}^{sat}$  to provide the first voltage supply, or the first voltage supply is 1.8 volts and the second voltage supply is a ground reference. It would have been obvious to one having ordinary skill in the art at the time the invention was made to optimum value of the voltage supply, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

15. Regarding to claim 9, 21, and 22, Lee et al. do not explicitly disclose the output node is coupled to an audio circuit or a power control circuit.

It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. EX parte Masham, 2 USPQ2d 1647 (1987).

16. Claim 7, is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claim 1 above, in view of Huijising et al. U.S. patent No. 5,486,790

Lee et al. do not disclose wherein the bias current is programmable to permit user selection of a bias current.

Huijising et al. teach an AB amplifier circuit having programmable control bias current (Col. 5 lines 49 – 50).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have bias current of Lee et al. 's amplifier programmable which has taught by Huijising et al for the purpose providing selection of bias currents (Col. 5 lines 49 – 50).

***Contact Information***

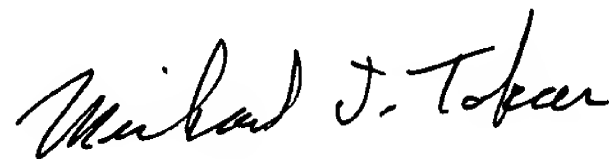
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

January 17, 2003



Michael Tokar  
Supervisory Patent Examiner  
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